In the Claims:

Please Amend Claim 17 as follows:

17. (AMENDED) A MOSFET device comprising:

an insulator layer overlying a semiconductor substrate;

polysilicon traces overlying said insulator layer;

a liner oxide layer overlying said polysilicon traces wherein said liner oxide layer covers sidewalls of said polysilicon traces on edges where source and drain regions are planned;

silicon nitride spacers on sidewalls of said polysilicon traces and overlying said liner oxide layer wherein said silicon nitride spacers have an L-shaped profile; and

an interlevel dielectric layer overlying said polysilicon traces, said silicon nitride spacers, and said liner oxide layer.

Please Amend Claim 21 as follows:

C2

21. (AMENDED) The device according to Claim 17 wherein said silicon nitride layer is formed by one of the group of: growing by thermal process and depositing by chemical vapor deposition.

[Please Amend Claim 22 as follows:]

22. (AMENDED) A MOSFET device comprising:

an insulator layer overlying a semiconductor substrate;

polysilicon traces overlying said insulator layer wherein said polysilicon traces comprise transistor gates;

a liner oxide layer overlying said polysilicon traces wherein said liner oxide layer covers sidewalls of said polysilicon traces on edges where source and drain regions are planned;

silicon nitride spacers on sidewalls of said polysilicon traces and overlying said liner oxide layer wherein said silicon nitride spacers have an L-shaped profile; and

an interlevel dielectric layer overlying said polysilicon traces, said silicon nitride spacers, and said liner oxide layer.

Please Amend Claim 25 as follows:

C3

25. (AMENDED) The device according to Claim 22 wherein said silicon nitride layer is formed by one of the group of: growing by thermal process and depositing by chemical vapor deposition.

[Please Amend Claim 26 as follows:]

26. (AMENDED) A MOSFET device comprising:

an insulator layer overlying a semiconductor substrate;

polysilicon traces overlying said insulator layer wherein said polysilicon traces comprise transistor gates;

a liner oxide layer overlying said polysilicon traces wherein said liner oxide layer covers sidewalls of said polysilicon traces on edges where source and drain regions are planned;

silicon nitride spacers on sidewalls of said polysilicon traces and overlying said liner oxide layer wherein said silicon nitride spacers have an L-shaped

profile and wherein said silicon nitride layer is formed by chemical vapor deposition; and

C3 Cont.

an interlevel dielectric layer overlying said polysilicon traces, said silicon nitride spacers, and said liner oxide layer.

REMARKS

Examiner F. Erdem is thanked for the thorough examination and search of the subject Patent Application. Claims 17, 21, 22, 25, and 26 have been amended.

All Claims are believed to be in condition for Allowance, and that is so requested.

Reconsideration of Claims 17-21 rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al (U.S. Patent 6,235,600) in view of Ding et al (U.S. Patent 6,153,472) is requested based on Amended Claims 17 and 21 on the following remarks.

As has been noted, Chiang et al fail to disclose the liner oxide layer 60 overlying the polysilicon trace 56. It is further